Evaluation of an Alternate Soft Charge Circuit for Diode Front End Variable Frequency Drives

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Abstract -- Variable Frequency Drives (VFDs) with diode rectifier front end are typically equipped with a resistor-contactor arrangement to limit the inrush current into the dc bus capacitors, thereby providing a means for soft charging the dc bus capacitors. Because of the mechanical nature of the magnetic contactor typically used in VFDs, there exists a concern for fatigue. In addition, during a brown out condition, typically the contactor remains closed and when the voltage recovers, the ensuing transient is often large enough to possibly cause unfavorable influence to surrounding components in the VFD. Many researchers and application engineers have thought about this issue and many are actively seeking non-mechanical solutions in a cost effective manner.

In this paper, a new topology to soft charge the dc bus capacitor is proposed. Other techniques that have been evaluated are also introduced. The relative advantages and disadvantages are discussed. Experimental tests to show the feasibility of the proposed idea is also provided.

***Index Terms*—Soft Charge Circuit, Inrush Current Limiter, Surge Current Limiter after Brown Out, Brown Out Condition.**

I. INTRODUCTION

Typically, in most Variable Frequency Drives (VFDs) that have a large DC bus capacitor filter, there exists a need for a circuit similar to a resistor-contactor arrangement to limit the inrush current into the capacitors, and thereby provide a means to soft-charge the dc bus capacitors (Fig. 1). Because of the mechanical nature of the contactor, the reliability of the VFD is adversely affected. Moreover, interrupting DC current under certain circumstances can deteriorate the integrity of contacts. Given these facts, the soft-charge circuit is perhaps one part of the drive that is due for some attention and improvement.

There have been suggestions of replacing the magnetic contactor (MC in Fig. 1(a)) with a semiconductor switch, as shown in Fig. 1(b). However, the semiconductor switch will require intelligent control and is associated with steady-state power loss.

Thyristor controlled rectifiers [1] have been used in VFDs as shown in Fig. 1(c). In this topology, the input rectifiers are replaced by thyristors. The triggering angle of the thyristors are controlled in such a manner that the dc bus capacitor charges up smoothly with no inrush. When a brown out occurs, the thyristor angle is such that it provides the maximum output voltage possible, similar to a typical diode bridge. When the voltage recovers after a brown out condition, the difference between the peak value of the input voltage and the dc bus voltage is large enough to force the triggering angle to increase and thereby reduce the high inrush current. This technique is well established and is used by some VFD manufacturers, but has the following issues:

- Needs six (or three) pack thyristor modules – can be expensive, especially for small sizes.
- Needs six (or three) gate-trigger circuits along with sensing and decision making logic. The trigger and logic circuits occupy space and are expensive.
- The thyristors cause voltage notching effect due to overlap phenomenon during commutation. This requires the use of input ac inductor to reduce the notching effect on other equipment. The addition of AC inductor occupies space and will be an added cost.

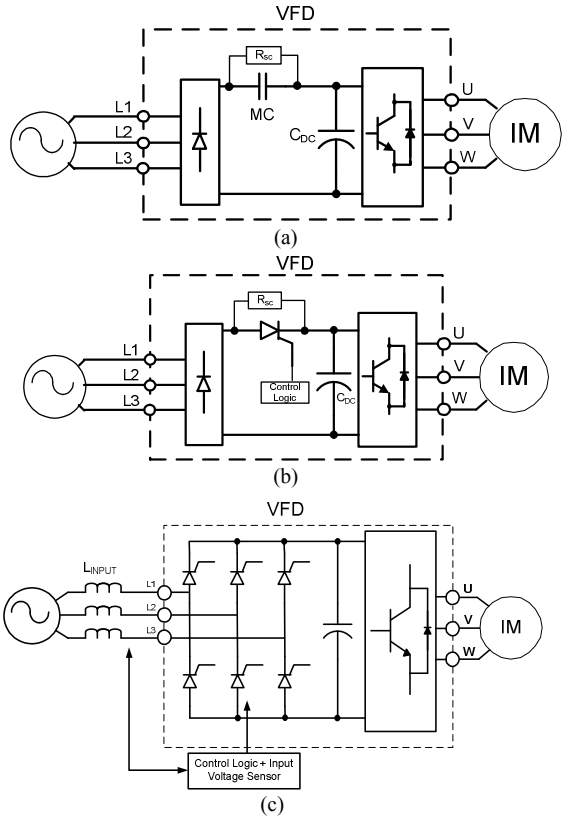


Fig. 1. Soft-charge circuit configuration, a. With Magnetic Contactor (MC), b. With Thyristor, c. Thyristor based rectifier [1].

This paper investigates alternate techniques to soft charge the dc bus capacitor. The target features are:

- No mechanical contactors;
- Should be able to handle brown out conditions in an efficient manner;
- Autonomous operation (without any control logic) to handle various power supply conditions;
- Unit should be compact and economical.

II. Study of Alternate Soft Charge Circuits

In this section, two alternate soft charge circuits that meet quite a few points in the target features are discussed. They are: a. Use of Magneto Resistive (MR) element; and b. Semi-converter type soft charge circuit.

A. Magneto Resistive (MR) Element based Soft Charger

One of the topology studied here includes the use of Magneto Resistive device (MR) that shows high resistance under the influence of large magnetic field and low resistance when the magnetic field resets to a lower level [2]. The MR element could be connected in series with the dc bus capacitor to soft charge it at start up or during the recovery time after a brown out condition. The circuit configuration is shown in Fig. 2(a) and the conceptual schematic in Fig. 2(b). In place of an E-I core based inductor, one can use a toroid and embed the MR element in the air-gap of the toroidal inductor. However, some important issues to consider while implementing an MR element based solution are as follows:

- Behavior of the MR element at elevated operating temperature should be considered. Since, most of the heat is produced in the air-gap of an inductor, placing an MR element in the air-gap needs careful engineering.
- Since rated load current has to pass through the MR element, this idea may be limited to small power due to the limitation of presently available material. When the rated current increases, the MR element can become large and placing it in the air gap may pose a problem.

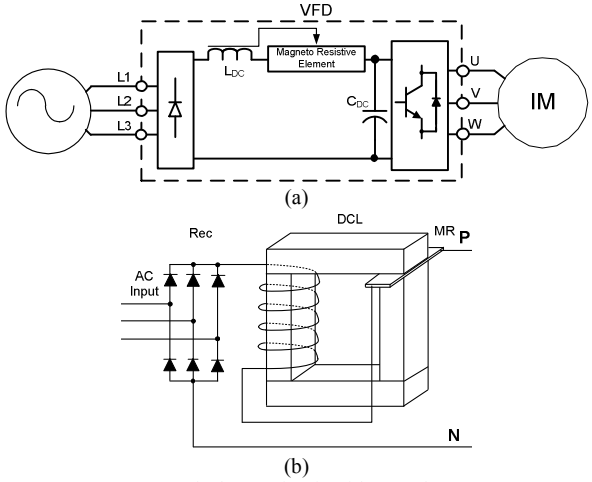


Fig. 2. Soft charge circuit with MR element.
a. Schematic, b. Conceptual implementation.

B. Semi-converter Topology based Charging [3]

In the semi-converter topology based charging, as the name suggests, a six-pulse rectifier is deliberately operated as a semi-converter by employing a wye connected auxiliary charging circuit as shown in Fig. 3. . The topology proposed here borrows the idea of a typical star-delta started used in conventional 3-phase ac motors. The dc bus capacitor is charged as a semi-converter at start and once the dc bus voltage reaches the steady state voltage dictated by the semi-converter, the full converter configuration is engaged, resulting in a second charge up period. Since the charging is carried out in two stages, the inrush current through the inductor, capacitor, and diode is well controlled with almost no stress. The switching from the semi-converter configuration to the full bridge configuration can either be dictated by level of dc bus voltage or by a timer. Both these methods have been simulated and found to yield acceptable results as shown in Figs 4 and 5.

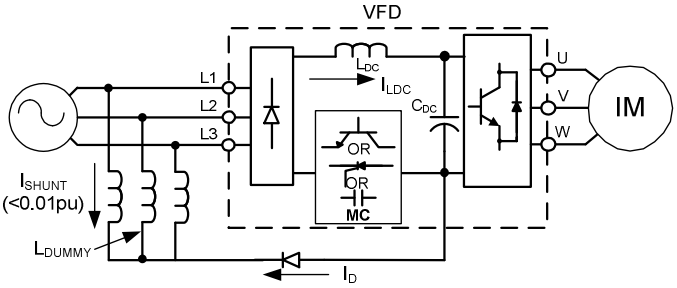


Fig. 3. Half-bridge to full bridge changeover topology that facilitates two-stage charging [3].

The value of the dummy inductor in Fig. 3 is chosen to be such that the resulting circulating current is about 0.01pu of the rated current. In the first of two strategies simulated here, the changeover from half-bridge configuration to full-bridge configuration is facilitated by detecting the level of the dc bus voltage across the main dc bus capacitors. The operating conditions assumed for simulation are as follows:

- The input line-line voltage is assumed to be 528V, 60Hz corresponding to 10% higher than nominal 480V;
- The dc link inductor is assumed to be 10% lower than its nominal value based on the manufacturer's specification;
- The dc bus capacitor is assumed to be 20% higher than its nominal value based on the manufacturer's specification;
- The equivalent series resistance (ESR) of the dc link inductor and the dc bus capacitor is determined from the manufacturer's datasheet;
- The parasitic resistance of the cable and the bus bars are assumed to be zero;
- The source is considered to have a short circuit capacity of 32,000 Amps (rms), with an X/R ratio of 5. For a 480V system, the value of the system inductance and resistance is computed to be 22.52μH and 1.7m-Ω;

- Power-up condition is simulated assuming no load is applied to the drive during power-up;
- The drive simulated is rated at 220-kW and the value of the dummy inductor chosen is 14mH.
- The dc bus voltage at which the half-bridge topology is changed over to the full-bridge configuration is selected to be 600Vdc.

Results of the simulation are given in Fig. 4.

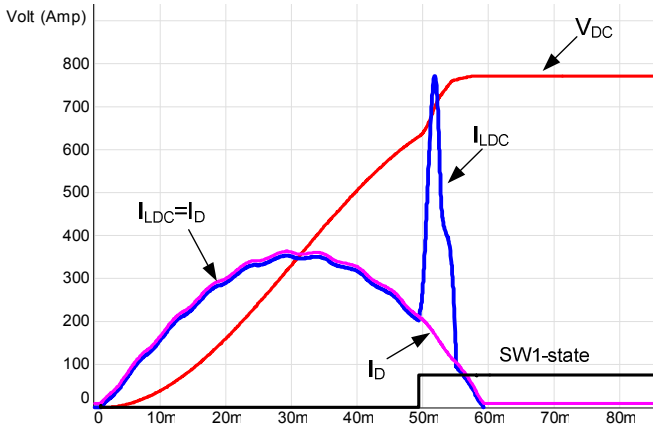


Fig. 4. Simulated results for the topology shown in Fig. 3. SW1 is activated based on level of dc bus voltage.

From the result shown in Fig. 4, it is interesting to see that even after switch SW1 is commanded to be closed, the large value of the dummy inductor keeps current flowing through the external diode D. During this period, two charging paths exist – one through D and the other through the lower section of the full-bridge rectifier diodes. In Fig. 4, the waveform for I_D has been shifted by 100A to distinguish it from I_{LDC}.

In Fig. 4, the observed peak surge current is 987A for a drive that has rated current of 515Arms. The maximum value of the dc bus voltage is seen to be 773V, which is well below the over voltage trip level of 850V.

Simulation results for the case when switch SW1 is closed after a pre-determined and fixed time is shown in Fig. 5.

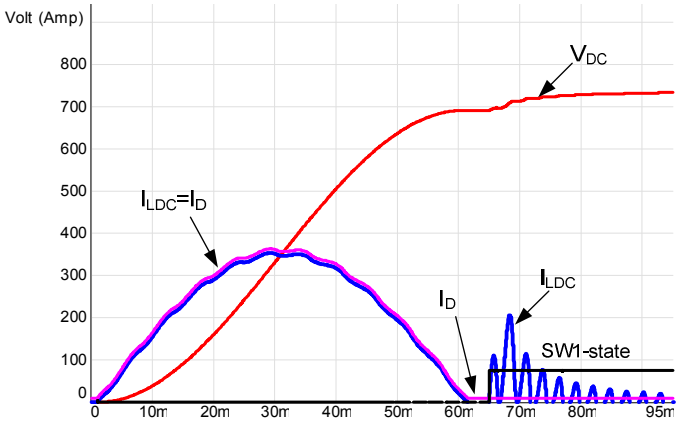


Fig. 5. Simulated results for the topology shown in Fig. 3. Here SW1 is shown activated after a pre-determined time of 65ms.

In Fig. 5, the observed peak surge current is 689A for a drive that has rated current of 515Arms. The maximum value of the dc bus voltage is seen to be 734V, which is well below the over voltage trip level of 850V.

Since the basic operation requires a logic circuit, this method was considered not to meet the target desired features. Moreover, a semiconductor switch has more losses than a mechanical contactor and this method can result in higher overall losses in the drive during normal operation. Given these important short comings, this technique was not pursued further. The need of a dummy inductor was yet one more drawback of this topology (Fig. 3).

III. Proposed Soft Charge Circuit

The proposed topology, shown in Fig. 6, meets most of the target desired features. A dc link inductor with a resistor assist circuit is employed to soft charge the dc bus capacitor [4]. The assist resistor also has a series thyristor.

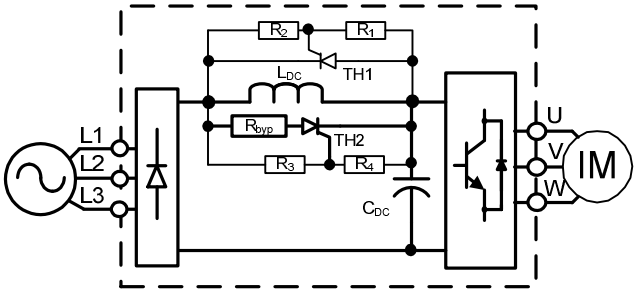


Fig. 6. Proposed circuit for soft charging the dc bus capacitor, employing two thyristors [4].

When AC power is applied to the circuit shown in Fig. 6, an inrush current begins to flow, assuming that the dc bus capacitor has no initial stored voltage. The inrush current is divided into two distinct paths. The first path is through the resistor-thyristor (TH2) combination and the second path is through the dc link inductor, L_{DC}. The current through the resistor-thyristor path is initially higher and quicker than that through L_{DC} since the inductor delays the build up of current through it. The dc bus capacitor starts to charge, with the resistor-thyristor combination providing as much charging as possible. The second charging path, through L_{DC}, creates a resonant circuit. Due to the nature of LC circuit, the voltage across the dc bus capacitor tends to increase over and above the peak value of the applied input AC voltage. At this time, the thyristor across L_{DC}, TH1, turns ON because it is forward biased and the gate voltage given by values of R1 and R2 exceeds the threshold gate voltage for TH1. In the meantime, TH2 turns OFF because the current through it falls below the holding current for TH2. In addition, the turning ON of TH1 causes the voltage across the inductor to start falling and eventually reverse biases thyristor TH2 and assures that TH2 is OFF. The inductor voltage linearly ramps to zero and gets clamped by TH1. The voltage across the DC bus capacitor stops increasing and eventually discharges into its discharge resistor to a level dictated by the input voltage condition.

The important aspect of the resistor-assist circuit cannot be

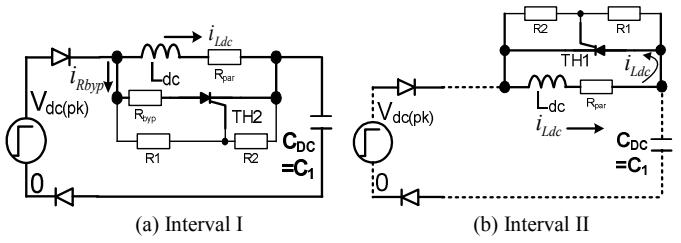
overlooked since the charging current flowing through L_{DC} is reduced due to the parallel resistor assist circuit. This reduces the stored energy in L_{DC}. It also lowers the saturation current requirement and makes the inductor physically smaller. Due to the LC nature of the circuit, the voltage across the capacitor is still higher than the peak value of the input voltage. The clamping circuit consisting of TH1 assures that the dc bus voltage is clamped to a safe value.

IV. Theory of Operation

The charging process, as discussed in the preceding paragraphs, is divided into two intervals – interval I and interval II. In the first interval, the resistor assist circuit with thyristor TH2 is primarily involved in charging up the dc bus capacitor. A charging current also flows through the main dc link inductor L_{DC}. When the voltage across the dc bus capacitor reaches the peak of the input applied voltage, the current through TH2 falls to zero and shuts it off. This marks the end of interval 1 and beginning of interval II. Depending on the relative value of R_{byp} and L_{DC} used, the start of interval II could see only current through the inductor. Eventually, when the voltage across the dc bus capacitor exceeds the gate threshold voltage for TH1, the clamping thyristor TH1 turns ON. Turning ON of TH1shorts out the dc link inductor and clamps the voltage across it to a value dictated by the parasitic resistance of the inductor and the forward voltage drop of thyristor TH1. This phenomenon also clamps the dc bus capacitor voltage to some safe level dictated by the forward voltage drop of thyristor TH1. Expressions for the charging current, final value of dc bus voltage and current through the two thyristors are derived next.

A. Interval I

Referring to Fig. 7(a), interval I of operation begins when the power is turned ON and the peak line-line voltage is applied to the inductor-resistor-capacitor combination and lasts till the voltage across the dc capacitor, v_{C1} reaches the peak input voltage and current through TH2 falls to zero. During interval I, two current paths exist – one through the bypass resistor and the other through the dc link inductor. At end of interval I, current through R_{byp} is zero since current through TH2 goes to zero.



(a) Interval I (b) Interval II

Fig. 7. (a). Equivalent circuit for interval I; (b). Equivalent circuit for interval II.

The expression for capacitor current ($i_{LDC} + i_{Rbyp}$) for zero initial capacitor voltage is:

$$V_{dc(pk)} = L_{DC} \cdot \frac{di_{LDC}}{dt} + \frac{1}{C_1}\int (i_{Rbyp} + i_{LDC})dt \quad (1)$$

$$i_{Rbyp} \cdot R_{byp} = L_{DC} \cdot \frac{di_{LDC}}{dt} \quad (2)$$

Differentiating (1) once and substituting (2) into the result yields the following equation:

$$\frac{d^2 i_{LDC}}{dt^2} + \frac{1}{R_{byp} \cdot C_1}\frac{di_{LDC}}{dt} + \frac{i_{LDC}}{L_{DC} \cdot C_1} = 0 \quad (3)$$

$$(D^2 + \frac{1}{R_{byp} \cdot C_1} D + \frac{1}{L_{DC} \cdot C_1}) \cdot i_{LDC} = 0 \quad (4)$$

$$D_1, D_2 = \frac{-1}{2R_{byp} \cdot C_1} \pm \sqrt{\frac{1}{4R_{byp}^2 \cdot C_1^2} - \frac{1}{L_{DC} \cdot C_1}} \quad (5)$$

As can be seen from (5), there are three possible solutions for the inductor current. They are: i. under-damped, ii. over-damped and iii. critically-damped. Operation of the unit that results in an over-damped system is not advisable since the current through the resistor would not have died before interval II starts and this can create higher current to circulate through TH1 in interval II. Such a situation is deliberately avoided and so will not be analyzed here.

1) Under-damped Case

In this case, $R_{byp}^2 > L_{DC}/(4 \cdot C_1)$. The expression for i_{LDC} can then be derived as follows:

$$i_{LDC} = A_1 e^{(\alpha + j\beta)t} + A_2 e^{(\alpha - j\beta)t} \quad (6)$$

$$\alpha = \frac{-1}{2R_{byp} \cdot C_1}; \beta = \sqrt{\frac{1}{L_{DC} \cdot C_1} - \frac{1}{4R_{byp}^2 \cdot C_1^2}} \quad (7)$$

$$i_{LDC} = e^{\alpha t}\{(A_1 + A_2)\cos(\beta t) + (A_1 - A_2) j \sin(\beta t)\} \quad (8)$$

At $t=0^+$, $i_{LDC(t=0^+)} = 0$; Substituting this condition yields:

$$(A_1 + A_2) = 0 \quad (9)$$

$$i_{LDC} = 2A_1 \cdot e^{\alpha t} \cdot j \sin(\beta t) \quad (10)$$

At $t=0^+$, since the initial voltage across the capacitor C1 is assumed to be zero, all the applied voltage appears across the dc link inductor-charge assist resistor combination. Using this condition, the value of A_1 and i_{LDC} are derived next:

$$L_{DC} \cdot \frac{di_{LDC}}{dt} = 2 \cdot L_{DC} \cdot A_1 e^{\alpha t} \cdot j \cdot (\alpha \cdot \sin(\beta t) + \beta \cdot \cos(\beta t)) \quad (11)$$

$$V_{DC(pk)} = 2 \cdot L_{DC} \cdot A_1 \cdot j \cdot \beta \quad (12)$$

$$2A_1 \cdot j = \frac{V_{DC(pk)}}{L_{DC} \cdot \beta} \quad (13)$$

$$i_{LDC} = \frac{V_{DC(pk)}}{L_{DC} \cdot \beta} \cdot e^{\alpha t} \cdot \sin(\beta t) \quad (14)$$

Since the dc link inductor and the assist resistor are in parallel when thyristor TH2 is conducting during interval I, the current through the assist resistor can be estimated by equating the voltage drop across the inductor to be same as that across the resistor. Once the current through the assist

resistor is estimated, the sum of the currents through the assist resistor and the dc link inductor can then be estimated, which will equal the actual charging current into the capacitor. Such an exercise is undertaken next:

$$i_{Rbyp} \cdot R_{byp} = L_{DC} \cdot \frac{di_{LDC}}{dt} \quad (15)$$

$$i_{Rbyp} = \frac{V_{DC(pk)}}{R_{byp} \cdot \beta} \cdot e^{\alpha t} \cdot (\alpha \cdot \sin(\beta t) + \beta \cdot \cos(\beta t)) \quad (16)$$

$$i_{C1} = i_{LDC} + i_{Rbyp} \quad (17)$$

$$= \frac{V_{DC(pk)}}{L_{DC} \cdot \beta} \cdot e^{\alpha t} \cdot \left(\sin(\beta t) + \frac{L_{DC}}{R_{byp}} \cdot (\alpha \cdot \sin(\beta t) + \beta \cdot \cos(\beta t)) \right) \quad (18)$$

Interval I ends when the current through the assist resistor decays to zero. Equating 16 to zero yields the end time ($t=t_1$) for interval I as follows:

$$i_{Rbyp} = 0 = \alpha \cdot \sin(\beta t) + \beta \cdot \cos(\beta t) \quad (19)$$

$$t_1 = \frac{\pi - \phi}{\beta};\ \phi = \tan^{-1}\left(\frac{\beta}{\alpha}\right) \quad (20)$$

2) Critically Damped Case

Critically damped case happens when $R_{byp}^2 = L_{DC}/(4 \cdot C_1)$. The physical interpretation is that in a critically damped system, the turning ON of TH1 coincides with the turning OFF of TH2. The expression for i_{LDC} can be derived by assuming the following characteristic for inductor current:

$$i_{LDC} = (A_1 + A_2 \cdot t) \cdot e^{-\alpha t} \quad (21)$$

$$\omega = \frac{1}{\sqrt{L_{DC} C_1}} \quad (22)$$

$$\text{At } t = 0^+, i_{LDC} = 0; \therefore A_1 = 0 \quad (23)$$

Again, at $t=0^+$, the initial voltage across the capacitor C1 is zero and all the applied voltage appears across the dc link inductor-charge assist resistor combination. Using this condition, the value of A_2 and i_{LDC} are derived next:

$$L_{DC} \cdot \frac{di_{LDC}}{dt} = L_{DC} \cdot (A_2 \cdot (1 - \omega t)) \cdot e^{-\alpha t} \quad (24)$$

$$\text{At } t = 0^+, L_{DC} \cdot \frac{di_{LDC}}{dt} = V_{DC(pk)} \ \therefore A_2 = \frac{V_{DC(pk)}}{L_{DC}} \quad (25)$$

$$i_{LDC} = \frac{V_{DC(pk)}}{L_{DC}} \cdot t \cdot e^{-\alpha t} \quad (26)$$

The current through the assist resistor can now be evaluated as done earlier by equating the voltage drops across the inductor and that across the assist resistor. This yields:

$$L_{DC} \cdot \frac{di_{LDC}}{dt} = V_{DC(pk)} \cdot (1 - \omega t) \cdot e^{-\alpha t} = i_{Rbyp} \cdot R_{byp} \quad (27)$$

$$i_{Rbyp} = \frac{V_{DC(pk)}}{R_{byp}} \cdot (1 - \omega t) \cdot e^{-\alpha t} \quad (28)$$

The sum of the currents through the dc link inductor and the assist resistor will yield the total charging current into the dc bus capacitor. For critically damped system, this current is estimated as follows:

$$i_{C1} = i_{LDC} + i_{Rbyp} \quad (29)$$

$$i_{C1} = V_{DC(pk)} \cdot e^{-\alpha t} \cdot \left(\frac{t}{L_{DC}} + \frac{(1 - \omega t)}{R_{byp}} \right) \quad (30)$$

Again, interval I ends when the current through the assist resistor decays to zero. Equating 28 to zero yields the end time ($t=t_1$) for interval I as follows:

$$i_{Rbyp} = 0 = (1 - \omega t_1) \quad (31)$$

$$t_1 = \frac{1}{\omega};\ t_1 = \sqrt{L_{DC} \cdot C_1} \quad (32)$$

B. Interval II

Referring to Fig. 7(b), interval II of operation begins when the current through thyristor TH2 falls to zero. This happens when the voltage across the dc bus capacitor C1 reaches the instantaneous maximum value of the applied line-line voltage. During this interval, depending on the relative value of L_{DC} and R_{byp}, thyristor TH1 eventually turns ON and clamps the voltage across the inductor L_{DC} to a value given by the forward voltage drop of thyristor TH1. The energy stored in the inductor is dissipated in the lumped parasitic resistance, R_{par}, comprising of the resistance of the windings of the dc link inductor, L_{DC} and the on-state resistance of TH1. The equation describing the current decay through the inductor is derived next.

$$0 = L_{dc} \cdot \frac{di_{Ldc}}{dt} + i_{Ldc} \cdot R_{par}; \quad (33)$$

$$i_{Ldc} = I_{LDC}(\text{at end of interval I}) \cdot (e^{\frac{-R_{par} t}{L_{dc}}}) \quad (34)$$

$$I_{LDC}(\text{at end of interval I}) = \frac{V_{DC(pk)}}{L_{DC} \cdot \beta} \cdot e^{\frac{\alpha(\pi - \phi)}{\beta}} \cdot \sin(\phi) \quad (35)$$

$$I_{LDC}(\text{at end of interval I}) = \frac{V_{DC(pk)}}{L_{DC} \cdot \sqrt{\alpha^2 + \beta^2}} \cdot e^{\frac{\alpha(\pi - \phi)}{\beta}} \quad (36)$$

$$i_{Ldc} = \frac{V_{DC(pk)}}{L_{DC} \cdot \sqrt{\alpha^2 + \beta^2}} \cdot e^{\frac{\alpha(\pi - \phi)}{\beta}} \cdot (e^{\frac{-R_{par} t}{L_{dc}}}) \quad (37)$$

For a critically damped system,

$$i_{Ldc} = \frac{V_{DC(pk)}}{\sqrt{L_{DC}/C_1}} \cdot e^{-1} \cdot (e^{\frac{-R_{par} t}{L_{dc}}}) \quad (38)$$

V. Test of Proposed Soft Charge Circuit

Power up and load tests were conducted using the circuit shown in Fig. 6. The details of the test setup are as follows:

1. Varispeed F7 drive — F7U4030 - 480V, 30kW, 60A
2. DC Link Inductor — L_{DC}= 0.9mH; I_{rated}= 60Arms
3. R_{byp} — 1-Ω
4. External SCRs — Series SCR (SKKT 250/16); I_{rated} = 250Arms; 1600V

5. Gate Trigger Circuit R_2=R_4= 900Ω.
R1= 62Ω; R3= 15.5Ω

6. Operating Condition i. Power-Up using 3-phase 480V, 60Hz AC supply;
ii. Load operation to 50hp

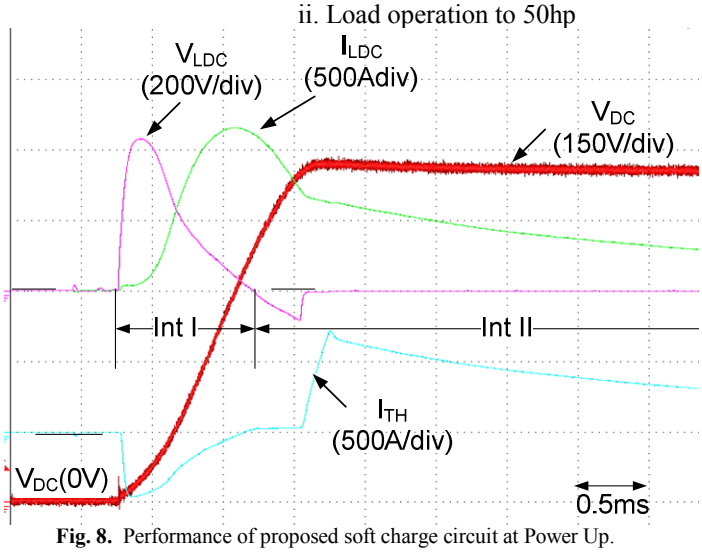


Fig. 8. Performance of proposed soft charge circuit at Power Up.

The various relevant parameters measured after power up are as follows:

Peak value of dc bus voltage: 745Vdc
Maximum dc inductor current: 1,159A
Maximum thyristor module current: 716A

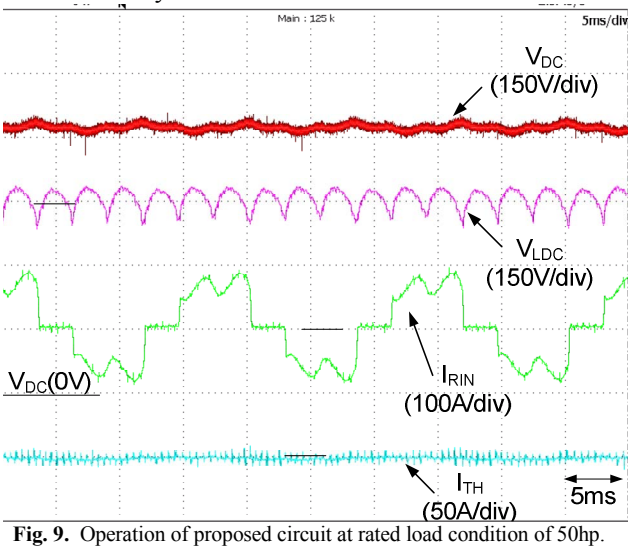


Fig. 9. Operation of proposed circuit at rated load condition of 50hp.

From the test results shown in Figs. 8 and 9, the following inferences can be made:

- The over voltage level for the drive used in the test is 850Vdc and since the maximum dc voltage observed was 745V, the unit did NOT fault out on over-voltage.
- The maximum value of the charging current into the capacitor was measured to be 1,230A, which is well below the maximum surge rating of 2,000A for the diode used.
- The peak thyristor current is well below 7,000A, which is the rating of the module used.
- The peak inductor current is 1,159A and the inductor does not show any sign of saturation since the core used has a very low relative permeability of 10.
- Under rated load condition, the voltage across the dc link inductor is small enough so as not to turn ON thyristors TH1 and TH2. This is clearly visible in Fig. 9 and it shows that the thyristors do not interfere during normal operation.

Brown-out tests were conducted next. The test plan was:

a. Power up the unit with 3-phase 480Vac (line-line) with the soft charge circuit.
b. Load the drive to half rated load condition.
c. Supply the drive with auxiliary power in parallel using a 3-phase auto transformer set at 380Vac (line-line).
d. Remove main supply power so that the load is supplied via the auxiliary power source at 380Vac.
e. After a brief interval of time, reapply power from the main AC source rated at 480Vac (line-line).

The schematic of the test setup is shown in Fig. 10 and the results are given in Fig. 11.

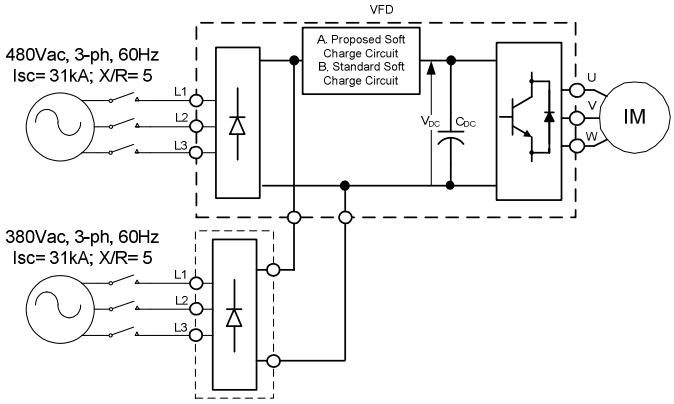


Fig. 10. Schematic of test set up to study performance during brown out condition. A. With proposed circuit, and B. With standard circuit that has magnetic-contactor and soft-charge resistor unit.

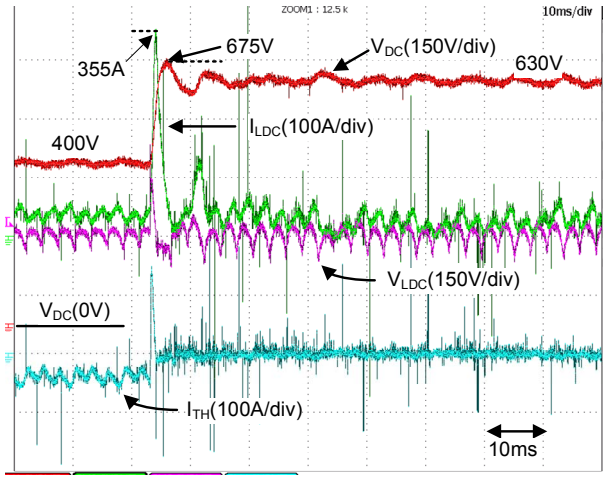


Fig. 11. Results obtained with proposed soft charge circuit in operation.

From the results shown in Fig. 11, the following inferences can be made:

1. The surge current resulting from the reapplication of rated voltage to the drive after a brown out condition is very well limited by the proposed soft charge circuit. This achieves the most important goal of the proposed circuit.
2. The over-voltage resulting from the reapplication of the rated voltage to the drive after a brown out condition is low and well below the over-voltage trip level for the drive. It is also well within the voltage tolerance level of the capacitors and IGBTs used. This shows that the clamping mechanism helps clamp the voltage to a safe level.
3. During a brown out condition, the current through the inductor increases significantly for the supplying the same load at lower dc bus voltage. The increased voltage drop across the inductor turns ON TH1 during the brown out period. This feature helps to keep the clamp circuit active and ready for the case when the voltage recovers as observed in Fig. 11 and clamps the capacitor voltage to a safe level.

VI. Conclusions

This paper presents an alternate soft charge circuit that is shown to be effective in soft charging the dc bus capacitor of a three-phase AC to DC rectifier circuit. Following are the important features of the proposed circuit:

- The voltage across the DC bus capacitor is limited by a clamp circuit that is active only when the voltage differential between the input of a dc link inductor and the dc bus capacitor exceeds a pre-determined value.
- A resistor assist circuit is employed to assist in soft charging the dc bus capacitor. The resistor assist part of the circuit is important since it prevents large current flowing through the dc link inductor that could potentially saturate the inductor. It also makes possible the realization of an inductor that is smaller in size and lower in cost.
- The proposed circuit does not need the addition of any external voltage or charging current sensing and decision making circuits. This makes the circuit very simple.
- Tests have shown that the proposed circuit performs satisfactorily during a voltage dip condition, as well.
- The other advantage of the proposed circuit is that it does away with mechanical contactor and associated time delay. The power loss aspect associated with power semiconductor replacement of mechanical contactor circuits is not present in the proposed method.
- An added advantage of employing an optimally sized dc link inductor as part of the soft charge circuit is that under normal operating condition, the input current THD is seen to be near 35%, and the input true power factor is close to 0.88.
- Employing the dc link inductor also helps reduce the total capacitance needed in the dc bus, since the current ripple is significantly reduced. Though this aspect has not been confirmed here, it is expected to result in saving of space and hence cost of the entire drive system.

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